Research Paper

ANALYSIS OF LOW NOISE AMPLIFIER IN 5 TO 9 GHZ RANGE

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ABSTRACT

In this paper a 5 to 9 GHz Low Noise Amplifier (LNA) with good gain and band pass property for Ultra Wide Band (UWB) applications designed using 0.18 \textmu m CMOS technology. Therefore, we proposed a wideband input network with band pass capability UWB LNA. It uses a CMOS amplifier with 0.18 \textmu m technology. We have achieved a good power gain and minimum noise figure for the core LNA.

KEYWORDS

Low-noise amplifier (LNA), Complementary metal–oxide semiconductor (CMOS), band pass, ultra wideband (UWB).
INTRODUCTION
The low noise amplifiers (LNA) are key components in the receiving end of the communication system and the performance is measured in a number of figures which are most notable while dynamic range, return loss and stability are examples. Signal received from the antenna is directly given to the low noise amplifier to reduce noise in external as well as internal noise of the circuit. In reference [1] we used two MOSFETs in cascode topology which has little effects with each other. The device parameters of MOSFETs connected in cascode topology can be design separately, with almost no trade-off [2, 3]. The topology requires more area with complexity increment. References [4-6] presented that LNA which are able to provide gain up to -15 dBm to input signal powers without adding much noise or degrading linearity. These all properties enable the wireless receiver to operate in hostile communication environments. During the design of low noise, the most important factors are low noise, forward gain, stability and matching. In this paper, we design a CMOS LNA using single stage inductive source degeneration topology with respect to noise optimization and impedance matching. Generally the cascoded topologies are used for the designing of CMOS LNA. Here we have used the inductive degeneration common source topology with active device biasing.

To increases the temperature sensitivity active devices used. Major applications of the LNAs [7-9] are to minimizing the noise as well as increase the signal power. Reference No [10] have proposed a model of the double-gate CMOS for double-pole four-throw RF switch design at nanometer technology, which is also an application for the LNA.

LNA DESIGN APPROACH
The 5 to 9 GHz CMOS UWB LNA, shown in fig 1, proposed here adopts a source-degenerated Cascode configuration. We use an LC input network for wideband operation with two new capacitors and for increasing the higher and lower band pass respectively. The load inductor is used series with the resistor helps to enhance the gain flatness. Buffer transistor with a purely resistive load is employed for testing purposes. Additional inductor is inserted to enhance the overall gain.

The overall gain of the LNA without an additional inductor $L_c$ is given by [22]

$$S_{21} = \frac{(1 + S_{11})v_{out}}{v_{in}}$$

$$= (1 + S_{11}) \frac{v'_{out}}{v_{in}} g_{m3(R_0||Z_o)} \quad (1)$$

Where

$$\frac{v'_{out}}{v_{in}} = \frac{g_m(1 - \omega^2 L_g C_{RH})}{\omega \sqrt{R_L}} \left[ R_L + j\omega L_c \right] \frac{1}{j\omega C_L} \quad (2)$$

With

$$(\omega) = \omega^4 L_g L_c C_f C_{RH} - j\omega^3 L_g L_c^2 g_m C_{RH}$$

$$- \omega^3 (L_g C_f + L_g C_{RH} + L_c C_t) + j\omega g_m L_2 + 1 \quad (3)$$
is the 50-Ω source resistance, $C_t = C_{gs1} + C_a$ and $CL$ is the total capacitance between the drain of the transistor $M_2$ and ground. $S_{11}$ is the reflection coefficient at the input port. From eq (1), it is seen that extra transmission zeros can be created when the following conditions are satisfied:

$$S_{11} = -1 \text{ or } \frac{v'_{\text{out}}}{v_{\text{in}}}$$  \hspace{1cm} (4)

In which means that the input impedance of the LNA is short circuit, and it occurs as the impedance $Z_R$, that is the impedance of the $L_1C_1\text{tank}$ in series with the capacitor $C_{RL}$ is equal to zero, where

$$Z_R(\omega) = \frac{1 - \omega^2 L_1 (C_{RL} + C_i)}{\omega C_L (1 - \omega^2 L_1 C_i)}$$  \hspace{1cm} (5)

By using (2), (4), and (5), the locations of transmission zeros can be predicted as

$$\omega_{BH} = \frac{1}{\sqrt{L_g C_{BH}}} \quad \omega_{HL} = \frac{1}{\sqrt{L_1 (C_{RL} + C_i)}}$$  \hspace{1cm} (6)

The overall gain of the circuit is increased by inserting an additional inductor as shown in the fig. Complete schematic of proposed LNA. With an additional inductor $L_c$, the increased value of the voltage gain is proportional to the inductance value of additional inductor $L_c$.

**C. Band pass capability**

The above ratiocination reveals that the additional capacitors and will bring about two transmission zeros to ameliorate the out-band performance. However, the band pass characteristics are restricted by the series resistance of the on-chip inductor. As seen from (6), higher and lower out-band transmission zeros are associated with the inductors and $L_1$, respectively. The values these component influence not only the zeros’ frequencies, but also the out-band suppression levels. Higher frequency out-band elimination efficiency is mainly determined by the impedance of the $L_gC_{RH}$ tank at the resonant frequency (i.e., the larger impedance, the superior out-band suppression). This way, the first step is to assign a larger to arrive at larger resonant impedance [20, Ch. 14]. With that a preferable power gain in the target frequency range can be procured contemporaneously by using a larger value of $L_g$. The impedance of input LC circuit produces one
parallel and one series resonance from which the lower transmission zero can be created. It is expectable that smaller impedance at the series resonant frequency will accomplish the superior out-band elimination efficiency.

IMPLEMENTATION AND SIMULATION

(A) Noise Figure

(B) Voltage Gain

(C) Power Gain

CONCLUSION

This paper proposed a UWB LNA configuration with band pass ability and presented the simulated results using the 0.18 µm CMOS process. By the use of an LC input network with additional capacitors extra transmission zeros are created and for improving the higher and lower out-band performances. Finally we have achieved gain enhancement and low power dissipation with an additional inductor.

REFERENCES


